The FPGA wireless communication block as the name suggests is responsible for managing the communication between the processing simulation and the sensing system. This block like any other, needs to meet certain requirements in order to ensure that data is transmitted and received in the intended manner. This block needs to meet the following requirements:

* The HC-05 Bluetooth module uses the UART protocol to communicate with the FPGA and therefore a UART transmitter component needed to be developed in FPGA to be able to send data to the Bluetooth module for transmission to the computer.
* The data is transmitted through SPI in bursts of 6 pieces orientation data and the ID of the IMU which the data belongs to. Because the maximum speed of the UART protocol is 115,200 bits per second [1] compared to 1,000,000 bits per second in the case of SPI, it makes the UART transmitter approximately 9 times slower than the SPI. For this reason, the FPGA wireless communication block needs to be able to store the data before transmission.
* The Processing simulation will control the rate of flow of data to avoid data being missed or misaligned when received by the computer. During previous design of this communication block it was found that when the FPGA wireless communication block controlled the rate of flow of data, information was missed and misaligned and therefore causing errors in converting data back to floating point in the simulation. To allow the simulation to control the rate of flow a receiver needed to be designed to enable communication from the computer to the sensing system.
* Because the UART protocol can only transmit data that is 8-bits wide, the received orientation data needs to be split from 16-bit to two 8-bit values for the protocol to be able to send the data.
* Since HC-05 uses the UART protocol, the block needs to comply with this protocol in order to transfer data for wireless transmission.
* Because the SPI works at 1,000,000 bits per second compared to UART at 115,200 bits per second [1], makes the UART protocol approximately 9 times slower than SPI. As established in the **‘Data Processing Block’**, Data is sent in bursts and therefore the this block needs a way of storing data before transmitting as to not miss any data.
* The UART protocol can only handle 8-bit wide data when transmitting and therefore this block will need to split the SPI data before transmitting.
* The block will need to be able to receive signals from the computer for data flow control purposes detailed in the **‘Processing Wireless Communication Block’**.

Data 
Request Signal 
FPGA Wireless Communication Block 
IMUn 
Orientation 
Data 
16-bit data 
Reset 
Timer 
Miso 
FPGA-STM32 
SPI 
CLKO 
data 
MOSI 
16-bit data 
Serial Data Line 
8-bit data 
d Reg 
UART 
Receiver 
8-bit data 
UART 
Tramsmitter 
Signal Line 
Data Request 
Dummy Byte 
IMUn 
Orientation 
Data 
Parallel Data Line 

Research links used to get information

[1] <https://learn.sparkfun.com/tutorials/serial-communication/all>